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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,052	CHO ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/6/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10 and 12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This communication is in response to Applicants' Remarks in Amendment filed July 6, 2006, which were persuasive in showing the formerly applied references fail to address the limitations of claims 9 and 14. Hence, a new rejection is presented.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-3, 5-8, 10, 12, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 5,871,562) in view of Weimer et al. (US 6,162,737), Havemann (US 5,565,384), and further in view of Tomita (US 6,806,549 B2).

Chang teaches a method for making FET stacked gate electrode structure (Abstract). The method comprises making an FET with self-aligned source/drain contacts having improved gate electrode profiles and improved sidewall spacers (column 4, lines 45-61), which reads on,

A method for fabricating a semiconductor device, the method comprising:

providing a semiconductor substrate having a device formation region (column 5, lines 5-10);

forming a gate on the device formation region of the semiconductor substrate, and forming source and drain regions in the device formation region of the semiconductor substrate adjacent respective sides of the gate, wherein the gate comprises a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer; forming an etch stop layer over the source region, the drain region and the sidewall spacers of the gate to obtain an intermediate structure (column 5, line 45 – column 6, line 58);

forming a planarized first interlayer insulating film over a surface of the intermediate structure (column 6, lines 45-58); and

and wherein the first interlayer insulating film is formed of silicon oxide by chemical vapor deposition (column 6, lines 17-27).

Chang also teaches, " . . . the FET . . . is now completed by depositing and patterning a metal layer **34** to form electrical contacts to the source/drain contact areas **23** (column 7, lines 19-22), which reads on,

forming respective contact pads by filling the self-aligned contact holes, **in claims 1 and 21**.

Chang further teaches,

wherein the gate is formed to further comprise a hard mask on a surface of the gate conductive layer (column 5, lines 36-38 and FIG. **2**), **in claim 2**;

wherein the sidewall spacer and the etch stop layer are formed of silicon nitride by chemical vapor deposition, and the first interlayer insulating film is formed of silicon oxide by chemical vapor deposition (column 6, lines 17-27), **in claim 3**;

further comprising forming a buffer layer on the source region and the drain region prior to forming the etch stop layer, and removing the buffer layer by wet etching after wet etching the etch stop layer (column 5, lines 16-20; column 6, lines 11-14 and 39-44, and column 7, lines 7-11), **in claims 5-7**;

wherein the buffer layer is formed of silicon oxide by thermal oxidation, (column 5, lines 16-18 and column 6, lines 10-13), **in claim 8**;

wherein the etch stop layer is formed of silicon nitride by chemical vapor deposition, (column 6, lines 17-27), **in claim 10**; and

wherein the wet etching of the etch stop layer comprises: removing oxide film remnants on the etch stop layer by wet etching by with an oxide etchant; and removing the etch stop layer using an oxide etching solution or a nitride etching solution, (column 7, lines 7-11), **in claim 12.**

Unlike the claimed invention, Chang fails to teach dry etching the first insulating layer until the etch stop layer over the source region, the drain region and the sidewall

spacers is exposed to form self-aligned contact holes in the first interlayer insulating over the source region and the drain region; and

wet etching the etch stop layer to remove the etch stop layer over the source region, the drain region and the sidewall spacers, **in claim 1**.

Weimer discloses selectively etching a BPSG insulative layer **34** with respect to a silicon nitride etch stop layer **32** by using a fluorocarbon as described in U.S. Pat. No. 5,286,344 (column 3, lines 16-22). Also in a similar embodiment, Weimer discloses, "After the selective etch to expose the etch stop layer **132**, . . . processing can include a silicon nitride etch, such as, for example, hot phosphoric acid" (column 8, lines 3-9). The aforementioned reads on, wet etching an etch stop layer.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chang by employing Weimer's selective etch method for the purpose of enhancing the etch selectivity by using a smaller etch stop layer without increasing the risk of over-etching as when using etch stop layers having a thickness of at least 2,000 angstroms to compensate for over etching of the etch stop layer in the selective etch (Weimer, column 6, lines 13-22).

Chang in view of Weimer further differs in failing to teach filling the self-aligned contact holes with conductive polysilicon, **in claims 1, 20, and 21**.

Havemann discloses depositing Ti/TiN/AlCu alloy, for example, in contact holes and list alternate examples of conductors as polysilicon (column 6, lines 20-27 and Table).

Since Havemann illustrates that a conductor comprising polysilicon is known, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chang in view of Weimer by using Havemann's conductor because it is seen as an alternate example without deviating from the nature of the invention (Havemann, column 7, lines 31-32).

Chang in view of Weimer and Havemann differ is failing to teach wherein the first interlayer insulating film is silicon oxide film formed by high-density plasma chemical vapor deposition, **in claim 1**.

Tomita discloses "A silicon oxide film (hereinafter called an "HDP oxide film") formed by means of, e.g., the high-density chemical vapor deposition (HDPCVD) method is taken as the plasma silicon oxide film" (column 4, lines 61-64).

Since Tomita illustrates forming silicon oxide film by HDPCVD) is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ Tomita's method of depositing an oxide layer because such method is used in the manufacturing of semiconductor devices (column 2, lines 59-61).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US '562) in view of Weimer (US '737), Havemann (US '384) and Tomita (US '549 B2) as applied to claim 1 above, and further in view of Lu (US 6,479,341 B1).

Chang in view of Weimer, Havemann, and Tomita differ in failing to teach wherein the buffer layer is formed of a mid-temperature oxide (MTO) by low pressure chemical vapor deposition.

Lu discloses, "A first insulator layer of silicon oxide **9**, is next deposited using LPCVD or PECVD procedures, at a temperature between about 200 to 600 °C (column 4, lines 16-18), which is formed of the same material, by the same method, and within the same temperature range as Applicants' MTO buffer as specified in the Specification [0020].

Since Lu illustrates forming an oxide layer, which is the same material as Applicants' buffer layer that is formed of a mid-temperature oxide, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chang in view of Weimer Havemann, and Tomita by using Lu's method of forming an oxide layer, is the same as Applicant's MTO buffer because such method is used effectively in a method of forming semiconductor devices (column 2, lines 18-23).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US '562) in view of Weimer (US '737), Havemann (US '384) and Tomita (US '549 B2) as applied to claim 1 above.

Chang in view of Weimer Havemann and Tomita differ in failing to teach wherein the oxide etching solution includes a concentration of diluted hydrofluoric acid (HF) having a density of 0.01 wt % through 0.001 wt %.

However, Chang illustrates the oxide etching solution, which includes hydrofluoric acid. (column 6, lines 59-64) is known. Hence it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to select any proportion of wt % of HF in the Chang reference, including the concentration range of wt

% of HF as claimed by Applicants, that would effectively accomplish the disclosed composition because it has been held that there is no invention where the difference in proportions is not critical and was ascertained by routine experimentation because the determination of workable ranges is not considered inventive. See In re Swain and Adams, 70 USPQ 412 (CPA 1946).

6. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US '562) in view of Weimer (US '737) Havemann (US '384) and Tomita (US 549 B2) as applied to claim 1 above.

Chang in view of Weimer, Havemann and Tomita differ in failing to teach wherein the density of phosphoric acid H_3PO_4 is 50 wt % through 80 wt %, **in claim 14.**

However, Weimer illustrates the nitride etching solution, which includes hot H_3PO_4. (column 8, lines 5-6) is known. Hence it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to select any proportion of wt % of H_3PO_4 in the Weimer reference, including the concentration range of wt % of H_3PO_4 as specifically claimed by Applicants the that would effectively accomplish the disclosed composition in a method of selectively etching silicon nitride, Weimer, column 8, lines 36).

7. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US '562) in view of Weimer (US '737), Havemann (US '384) and Tomita (US '549 B2) as applied to claim 1 above, and further in view of Kim et al. (US-PGPUB 2002/0064968 A1).

Chang in view of Weimer Havemann and Tomita differ in failing to teach wherein the buffer layer is removed using an etching solution including ammonium hydroxide (NH_3OH), hydrogen peroxide (H_2O_2), and deionized water, **in claim 16**;

wherein the etching solution includes a concentration of ammonium hydroxide (NH_4OH) ranging form about of 0.1 wt % through 1.0 wt %, **in claim 17**;

wherein the etching solution includes a concentration of hydrogen peroxide (H_2O_2) ranging form about of 4.0 wt % through 7.0 wt %, **in claim 18**;

wherein the wet etching is performed at a temperature of 30°C through 80°C, **in claim 19**.

Kim teaches wet etching hole spacers formed of a layer of a MTO (which is the same material as applicants' buffer layer) using a mixture of NH_4OH and H_2O_2 to remove native oxides formed on the surface of the substrate as well as to remove contaminants remaining in the contact holes ([0030, line 6 –0031, line 6]). Also since Kim is silent as to the etching temperature, then one can assume that the etching is carried out at standard operating conditions of 25°C and 1 atm.

Since Kim illustrates removing a buffer layer using applicants' specific combination of NH_4OH and H_2O_2 is known, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to select any proportion of wt% and temperature in the Kim reference that would effectively accomplish the disclosed composition because it has been held that there is no invention where the difference in proportions is not critical and was ascertained by routine experimentation

because the determination of workable ranges is not considered inventive. See In re Swain and Adams, 70 USPQ 412 (CPA 1946).

Response to Arguments

8. Applicant's arguments, see Remarks, filed 7/6/2006, with respect to the rejection(s) of claim(s) 1-21 under Chang (US '562) in view of Weimer (US '737), and Havemann (US '384) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chang (US '562) in view of Weimer (US '737), Havemann (US '384) and Tomita (US '549 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

ltue

August 31, 2006

NADINE NORTON
SUPERVISORY PATENT EXAMINER
ART UNIT 1765